PATENT **Docket No. AUS920010547US1**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTORS: **A.E. Mericas**

APPLICATION NO. **09/931,308**

FILED: **August 16, 2001**

TITLE: **EXTENDING WIDTH OF PERFORMANCE MONITOR COUNTERS**

Examiner: J. West
Art Unit: 2857
6805

CERTIFICATE OF MAIL

I hereby certify that this paper is being deposited with the U.S. Postal Service as First Class Mail, postage prepaid, in an envelope addressed to Commissioner for Patents, MAIL STOP APPEAL BRIEF-PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450, Attention: Board of Patent Appeals and Interferences on March 1, 2005.

Lynn M. White

Commissioner for Patents
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Attention: Board of Patent Appeals and Interferences

APPELLANTS' BRIEF

This brief is in furtherance of the Notice of Appeal filed in this case on December 21, 2004.

This brief is transmitted in triplicate.

1. REQUIRED FEE

The requisite fee ($500.00) set forth in §1.17(f) is authorized to be charged to Deposit Account No. 09-0447.

2. REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation, having its principal place of business at New Orchard Road, Armonk, New York 10504. Accordingly, International Business Machines Corporation is the real party in interest.

3. RELATED APPEALS AND INTERFERENCES

The appellant, assignee, and the legal representatives of both are unaware of any other appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

4. STATUS OF CLAIMS

A. Claims canceled: 3, 10, and 15

B. Claims withdrawn from consideration but not canceled: 6 and 7

C. Claims pending: 1, 2, 4, 5, 8, 9, 11-14, 16 and 17

D. Claims allowed: none

E. Claims rejected: 1, 2, 4, 5, 8, 9, 11-14, 16 and 17

F. Claims appealed: 1, 2, 4, 5, 8, 9, 11-14, 16 and 17

Appealed claims 1, 2, 4, 5, 8, 9, 11-14, 16 and 17 as currently pending are attached as Appendix A hereto.

5. STATUS OF AMENDMENTS

No amendment after final was filed in the present case. A Reply under 37 C.F.R. §1.111 was filed on May 6, 2004 and resulted in the final Office Action appealed herein. A Notice of Appeal was filed on December 21, 2004 and was received in the USPTO on December 27, 2004.

6. SUMMARY OF THE CLAIMED INVENTION

The present invention is a performance monitor having plural performance monitor counters (PMC's) and at least one monitor mode control register (MMCR), where each PMC is controlled by the MMCR to pair or group the PMCs so that the overflow from one PMC can be directed to its pair/group. In a preferred embodiment of the present invention, when the number of events to be monitored is less than the number of counting elements, the MMCR groups the PMCs by dividing the number of available PMCs (counting elements) by the number of events being monitored by the PMCs; taking the integer portion of the result of this dividing step and assigns a number of PMCs, equal to that integer, to each of the events to be counted; and, if there are any remaining unassigned PMCs, assigning the unassigned counting elements to at least one of the events. Basically, what this means is that when the PMCs are grouped,

they are divided up as evenly as possible, and then any remainder is applied to at least one of the events to be counted.

7. U.S. Patent No. 5,557,548 to Gover et al.

U.S. Patent No. 5,557,548 to Gover et al. ("Gover") teaches a method and system which monitors specified events among the number of events within a data processing system. An MMCR allows control over which PMCs are used to monitor which events, and this control enables the ability of certain of the PMCs to be used for overflow of other PMCs.

8. U.S. Patent Application Publication No. US2002/0026524 to Dharap

U.S. Patent Application Publication No. US 2002/0026524 to Dharap teaches, in the context of the limited ability to display data on the small screen of a wireless device, a method for converting a list of data to a format displayable on a limited display area. The list is sorted, grouped into sets, and then a set identifier is displayed which can be accessed by the user if they want more detail. For example, in an address list, instead of displaying McBurney, Michaels, Moorhead, etc., there is a single display of letters of the alphabet, and a user would select "M" to go into more detail if desired.

Of relevance to the present invention is the teaching in Dharap of granuralizing the list when the maximum number of available entry locations is less than the number of entries on the list. Dharap divides the total number of table entries by the number of

available entries, and then displays an abbreviated list as a WAP page on a cellular phone.

9. ISSUES

A. ISSUE INVOLVING CLAIMS 1, 2, 4, 5, 8, 9, 11-14, 16 and 17

1. Whether Dharap, which is directed to reducing the number of entries displayed on a wireless device using a division process, is analogous art with respect to the division of entries in a performance monitor.

2. Whether the combination of Gover and Dharap as suggested by the Examiner suggests the claimed invention.

10. GROUPING OF CLAIMS

A. Claims 1, 2, 4, 5, 8, 9, 11-14, 16 and 17 stand or fall together.

11. ARGUMENT

A. Dharap is Non-Analogous Art with Respect to the Claimed Invention

Applicants respectfully traverse the rejection of the claims based on a proposed combination of Gover and Dharap as being an improper reliance on non-analogous art. The Dharap reference cited by the Examiner has nothing whatsoever to do with the division of PMCs among events being monitored by PMCs, and the Examiner has

provided nothing in support of a contention that a person of ordinary skill in the field of PMCs would look to the field of cellular telephone displays to solve the problem of how to divide up the allocation of PMCs when the number of events to be monitored by the PMCs is less than the number of available PMCs.

Turning to the teachings contained in Dharap, Dharap is directed to a method for converting a list of data to a format suitable for display and manipulation in a limited display area (e.g., the display screen on a cellular phone). Dharap is classified for publication in U.S. Class 709, Subclass 236, which is for ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MULTICOMPUTER DATA TRANSFERRING, computer-to-computer protocol implementing, computer-to-computer data framing.

1) <u>The Examiner has not Met the Two-Part Deminski Test</u>

In In re Deminski, 796 F.2d 436, 230 U.S.P.Q. 313 (Fed.Cir. 1986) the Federal Circuit adopted a two-step test for determining whether particular references are within the appropriate scope of the art, and this test has been repeatedly relied upon to make this determination in subsequent cases. See, for example, In re Clay, 966 F2d. 656, 23 U.S.P.Q.2d 1058 (Fed.Cir. 1992); Wang Laboratories, Inc. v. Toshiba Corp., 993 F.2d 858, 26 U.S.P.Q.2d 1767 (Fed.Cir. 1993); and In re Oetiker, 977 F.2d. 1443 (Fed.Cir. 1992). See also MPEP 2141.01(a).

The two-part Deminski test requires that (1) a determination be made as to whether the reference is within the field of the inventor's endeavor, and (2), assuming

the reference is outside that field, a determination be made as to whether the reference is reasonably pertinent to the particular problem with which the inventor was involved. In the present circumstances, neither test is met; thus, the references are not analogous art that can be combined to determine the patentability of the claims.

2) Dharap is Not Within the Field of the Inventors Endeavor

Clearly, Dharap is not within the field of the inventor's endeavor herein. The subject invention is directed to the field of performance monitoring within a data processing system. Recognizing that interrupts could not be used during initial hardware testing of a processor in the data processing system, or when the processor was executing time-sensitive code, the inventor herein developed a novel process for increasing the available width of PMCs during the initial hardware testing of the processor or when the processor is executing time-sensitive code that cannot be interrupted.

Dharap has nothing to do with processor design, performance monitoring, or extending the width of PMCs in a processor. The endeavor of Dharap is to enable the display of data on a small screen in a manner that is easy for a user of the small screen to use. This is clearly outside the field of endeavor of the inventor of the present invention.

3) Dharap is Not Reasonably Pertinent to the Particular Problem that the Inventor Solves

Since Dharap lies outside the field of the applicants' endeavor, the issue becomes whether the reference is reasonably pertinent to the particular problem with which the inventor was concerned. As noted above, the claimed invention is aimed at solving problems associated with the fact that interrupts could not be used during initial hardware testing of a processor in a data processing system, or when the processor was executing time-sensitive code. The applicant identified this problem and solved it by utilizing the present claimed structure.

A reference related to a displaying data on the small screen of a cellular telephone has no reasonable pertinence to solving the problem of an inability to use interrupts in certain situations involving hardware testing of a processor or the execution of time-sensitive code, problems that are solved by the present invention. One skilled in the art would not look to cellular telephone displays to solve such problems,

Furthermore, there is no reasonable basis for one skilled in the art attempting to solve "interrupt problem" to turn to display screens of small hand-held devices in an attempt to solve such a problem. Display screens have nothing to do with interrupts; they merely display data that is useful to a user of the display screen.

Therefore, since Dharap is not reasonably pertinent to the interrupt problem, it is not analogous art according to the pertinent case law and MPEP 2141.01(a). Accordingly, the Dharap reference should be removed form consideration herein and the claims allowed.

B. The Cited Art Does Not Teach or Suggest the Claimed Invention

The Examiner has not Established a *prima facie* Case of Obviousness

As set forth in the MPEP:

> To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings.
> MPEP 2143

As noted above, the present invention is directed to a particular method, system, and computer program product for calculating the division of plural PMCs among events being monitored by the PMCs. Applicant acknowledges that the present invention utilizes the control concept taught by Gover. However, the present invention improves upon the functionality of Gover by enabling the MMCR to calculate the optimal division of the PMCs among the events being monitored, when there are fewer events than PMCs. This division calculation is explicitly claimed in all of the independent claims, and thus is also claimed in all of the dependent claims.

The addition of Dharap does not teach the claimed elements, and does not provide a suggestion of a modification to achieve the claimed result. Dharap merely teaches that the display of data on a small display screen can be modified in a useable way to display less than the total of the data desired to be displayed, when needed. Since neither Dharap nor Gover teach or suggest these claimed elements, it is submitted that the present invention patentably defines over Gover and Dharap, both alone and in combination. Accordingly, each of the independent claims, and all claims

depending therefrom, patentably define over Gover and Dharap and are in condition for allowance.

The Board is respectfully requested to reconsider and withdraw the rejection of claims 1, 2, 4, 5, 8, 8, 11-14, 16 and 17under 35 U.S.C. §103.

12. CONCLUSION

For the foregoing reasons applicants respectfully request this Board to overrule the Examiner's rejections and allow claims 1, 2, 4, 5, 8, 9, 11-14, 16 and 17.

Respectfully submitted:

3/1/05
Date

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APPENDIX A

CLAIMS INVOLVED IN THIS APPEAL:

1. (Previously presented) A method for monitoring the occurrences of one or more events related to the operation of a processor, said processor including a performance monitor having a plurality of counting elements, said method comprising the steps of:

identifying the number of events to be counted by said performance monitor;

identifying the number of counting elements available to count incidences of said events; and

assigning at least two of said counting elements to serially count incidences of at least one of said events, wherein when the number of events to be counted is less than the number of counting elements available to count incidences of said events, said assigning step comprising at least the steps of:

dividing the number of available counting elements by the number of events to be counted;

in a first assignment step, assigning a number of counting elements, said number equal to the integer resulting from said dividing step, to each of said events to be counted; and

in a second assignment step, assigning any unassigned counting elements to at least one of said events.

2. (Original) A method as set forth in claim 1, wherein said performance monitor further includes at least one control element, said control element performing said steps of identifying the number of events, identifying the number of counting elements, and assigning of said counting elements.

3. (Canceled)

4. (Previously presented) A method as set forth in claim 2, wherein said assigning step further comprises at least the steps of:

determining the historical frequency of occurrence of incidences of said events to be counted; and

assigning said available counters to said events to be counted based upon said determined historical frequency.

5. (Previously presented) A method as set forth in claim 2, wherein said counting elements each comprise a performance monitor counter, and wherein each control element comprises a monitor mode control register.

6. (Withdrawn) A performance monitor for monitoring the occurrence of incidences of one or more events related to the operation of a processor, comprising:

at least one monitor mode control register; and

a plurality of performance monitor counters operatively connected to said monitor mode control register, said monitor mode control register grouping said performance monitor counters so that when one of said performance monitor counters reaches capacity in connection with the counting incidences of a first of said events, a second of said performance monitor counters begins counting subsequent incidences of said first of said events.

7. (Withdrawn) A performance monitor for monitoring the occurrence of incidences of one or more events related to the operation of a processor, comprising:

at least one control element; and

a plurality of counting elements operatively coupled to said control element, said control element grouping said counting elements so that when one of said counting elements reaches capacity in connection with the counting of incidences of a first of said events, a second of said counting elements begins counting subsequent incidences of said first of said events.

8. (Previously presented) A computer program product in a computer-readable medium for monitoring the occurrences of one or more events related to the operation of a processor, said processor including a performance monitor having a plurality of counting elements, said computer program product comprising:

first instructions for identifying the number of events to be counted by said performance monitor;

second instructions for identifying the number of counting elements available to count incidences of said events; and

third instructions for assigning at least two of said counting elements to serially count incidences of at least one of said events, wherein when the number of events to be counted is less than the number of counting elements available to count incidences of said events, said third instructions for assigning include at least:

fourth instructions for dividing the number of available counting elements by the number of events to be counted;

fifth instructions for assigning a number of counting elements, said number equal to the integer resulting from the execution of said fourth instructions, to each of said events to be counted; and

sixth instructions for assigning any unassigned counting elements to at least one of said events.

9. (Original) A computer program product as set forth in claim 8, wherein said performance monitor further includes at least one control element, said control element providing said first, second, and third instructions.

10. (Canceled)

11. (Previously presented) A computer program product as set forth in claim 9, wherein said third instructions further comprise at least:

seventh instructions for determining the historical frequency of occurrence of incidences of said events to be counted; and

eighth instructions for assigning said available counters to said events to be counted based upon said determined historical frequency.

12. (Original) A computer program product as set forth in claim 9, wherein said counting elements each comprise a performance monitor counter, and wherein each control element comprises a monitor mode control register.

13. (Previously presented) A system for monitoring the occurrences of one or more events related to the operation of a processor, said processor including a performance monitor having a plurality of counting elements, said system comprising:

means for identifying the number of events to be counted by said performance monitor;

means for identifying the number of counting elements available to count incidences of said events; and

means for assigning at least two of said counting elements to serially count incidences of at least one of said events, wherein the number of events to be counted is less than the number of counting elements available to count incidences of said events, said means for assigning comprising at least:

means for dividing the number of available counting elements by the number of events to be counted;

means for assigning a number of counting elements, said number equal to the integer resulting from operation of said dividing means, to each of said events to be counted; and

means for assigning any unassigned counting elements to at least one of said events.

14. (Original) A system as set forth in claim 13, wherein said performance monitor further includes at least one control element, said control element identifying the number of events, identifying the number of counting elements, and assigning of said counting elements.

15. (Canceled)

16. (Previously presented) A system as set forth in claim 13, wherein said assigning means further comprises at least:

means for determining the historical frequency of occurrence of incidences of said events to be counted; and

means for assigning said available counters to said events to be counted based upon said determined historical frequency.

17. (Original) A system as set forth in claim 13, wherein said counting elements each comprise a performance monitor counter, and wherein each control element comprises a monitor mode control register.